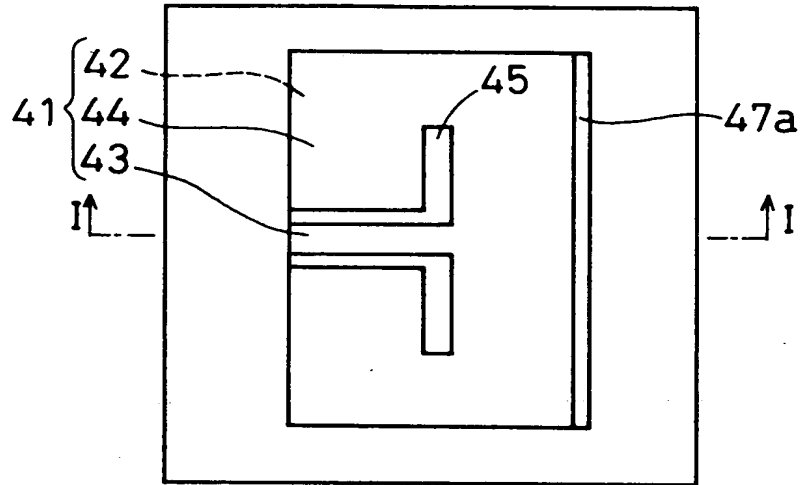
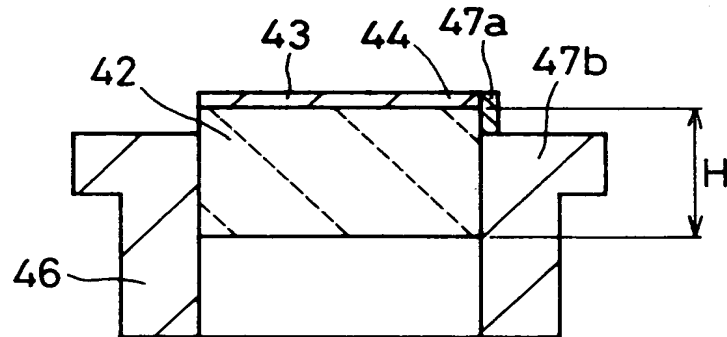


**FIG. 1A**



**FIG. 1B**



**FIG. 1C**

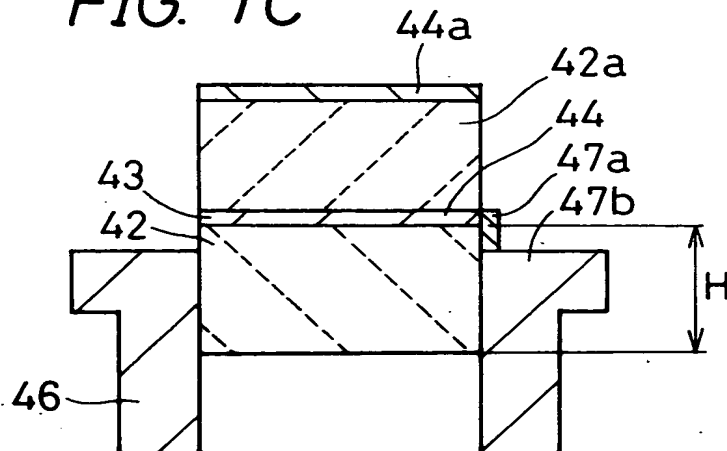


FIG. 2A

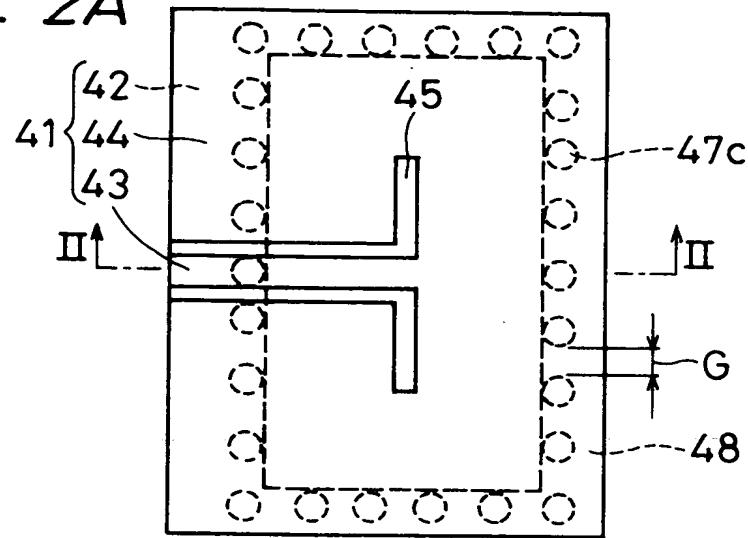


FIG. 2B

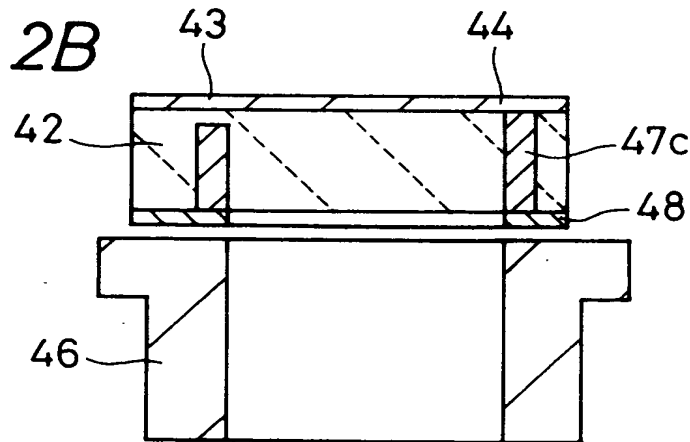


FIG. 2C

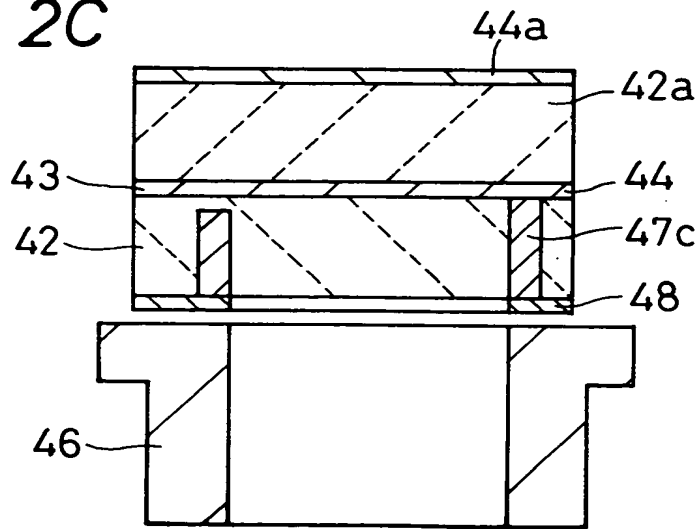


FIG. 3A

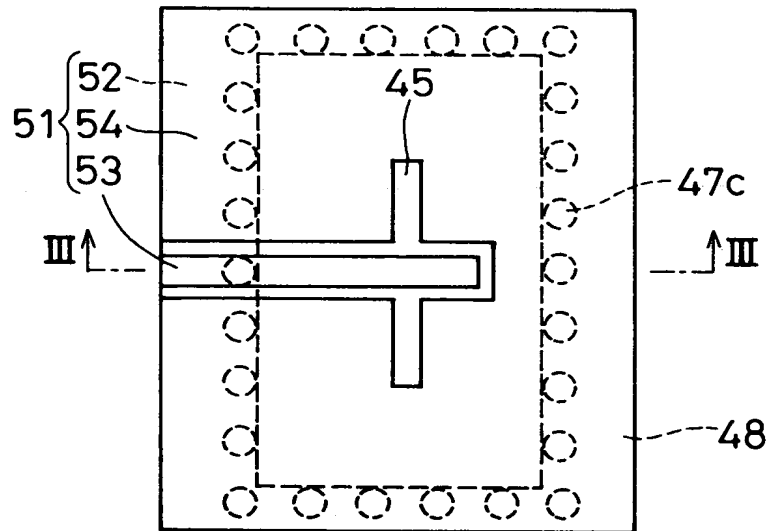


FIG. 3B

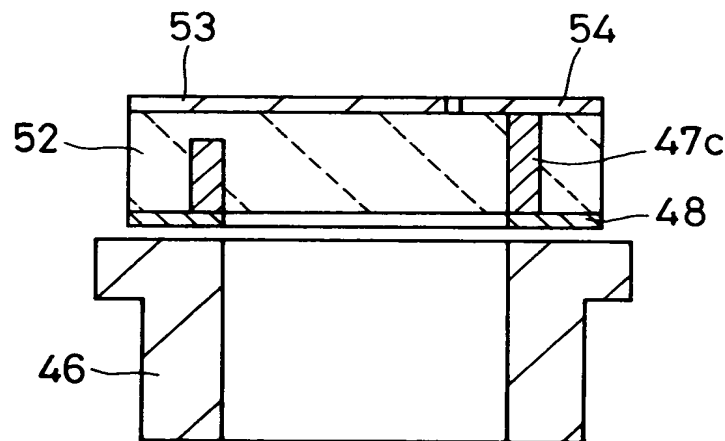


FIG. 4A

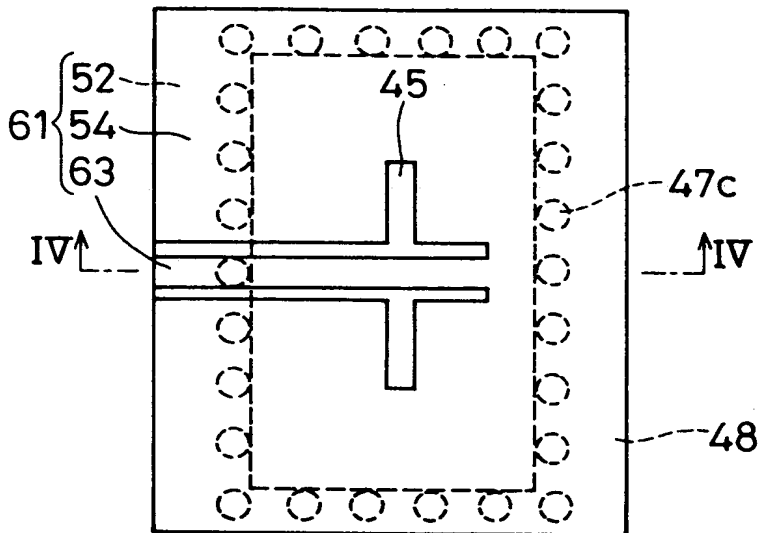
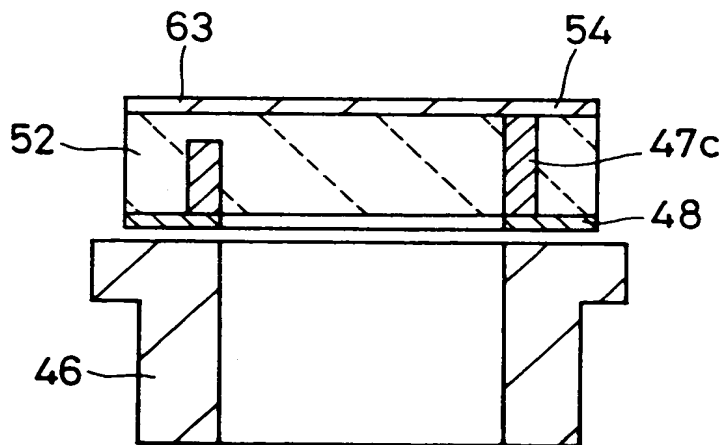
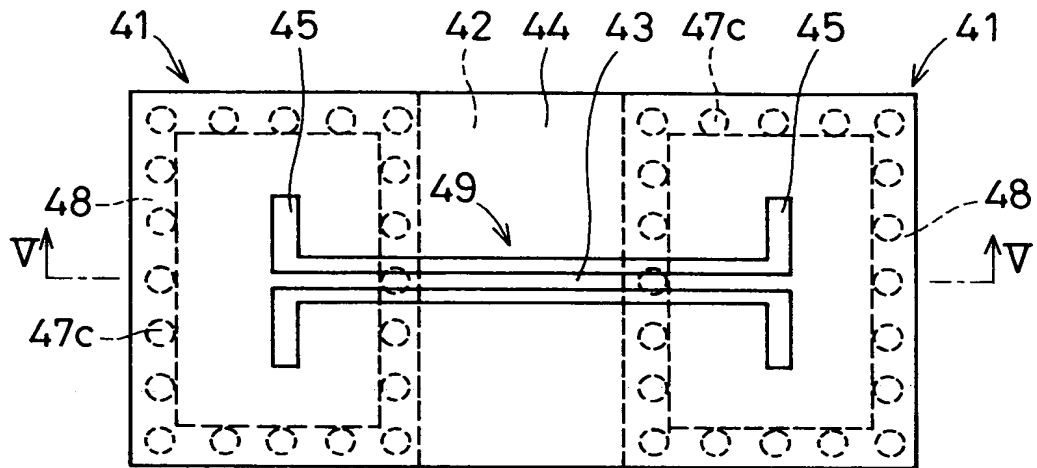


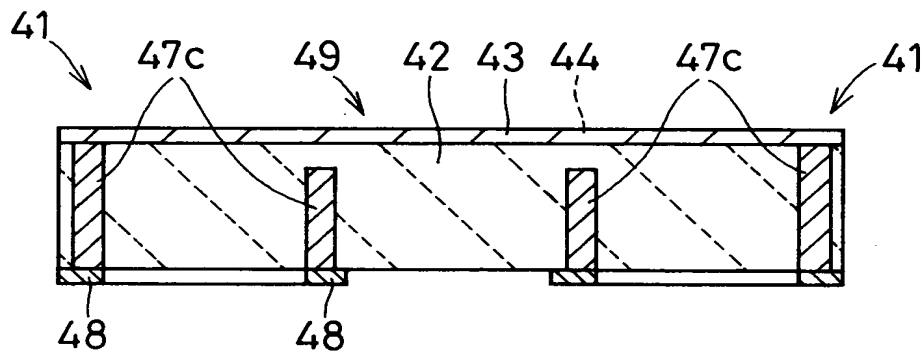
FIG. 4B



**FIG. 5A**



**FIG. 5B**



**FIG. 5C**

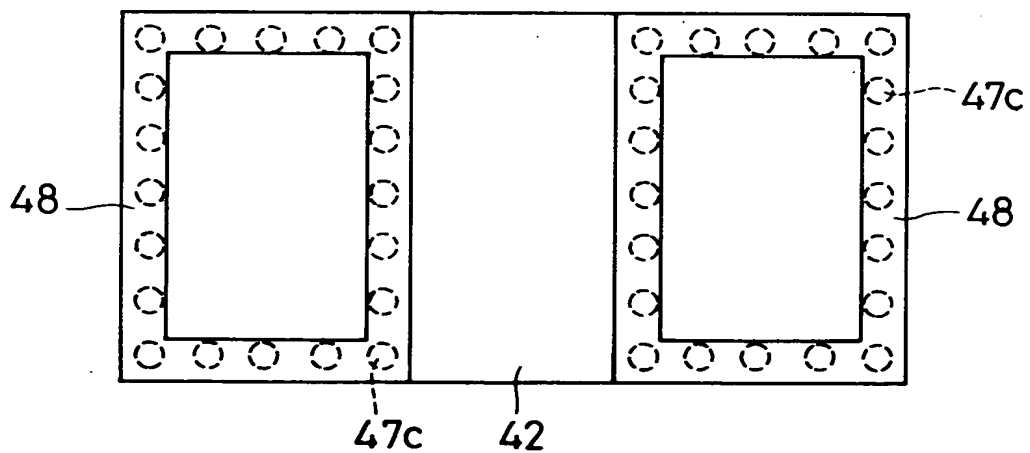
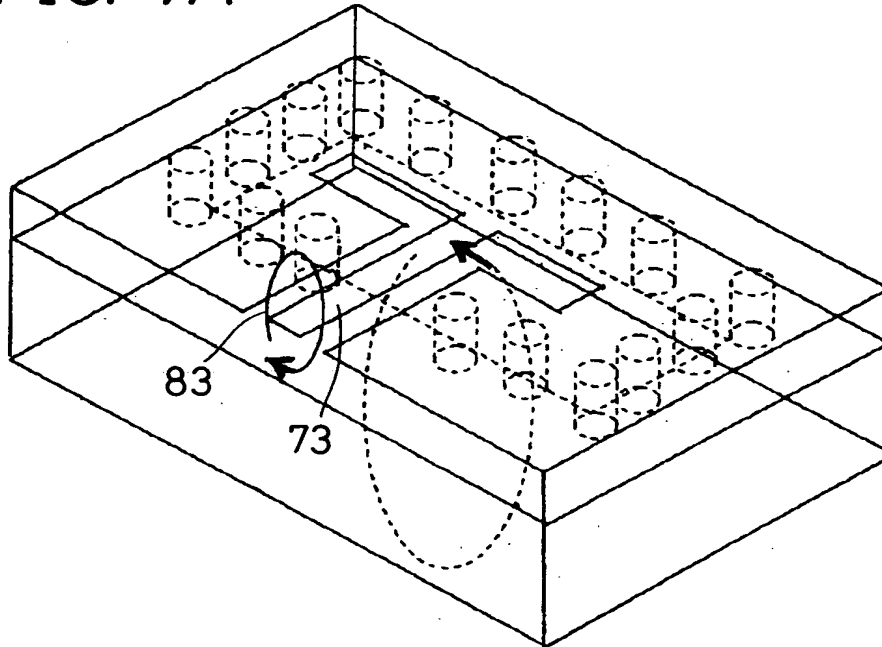
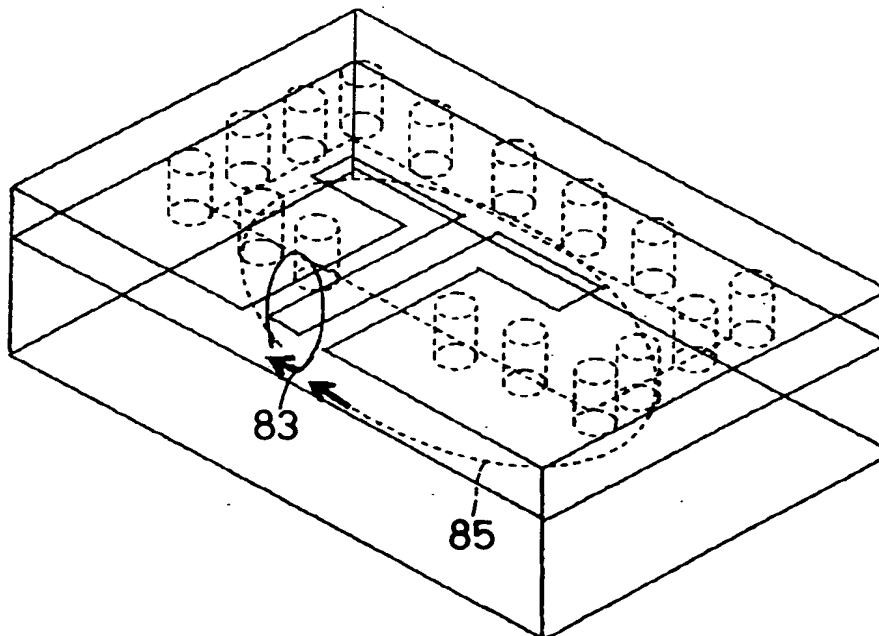


Fig. 1 is a schematic diagram of a semiconductor device. It shows a rectangular substrate with a central rectangular region containing a complex, interlocking pattern of solid lines. This central region is surrounded by a dashed rectangular border. The entire device is enclosed within a larger rectangular frame. Various components are labeled with numbers and letters: 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, and VI. Arrows indicate electrical connections or signals.

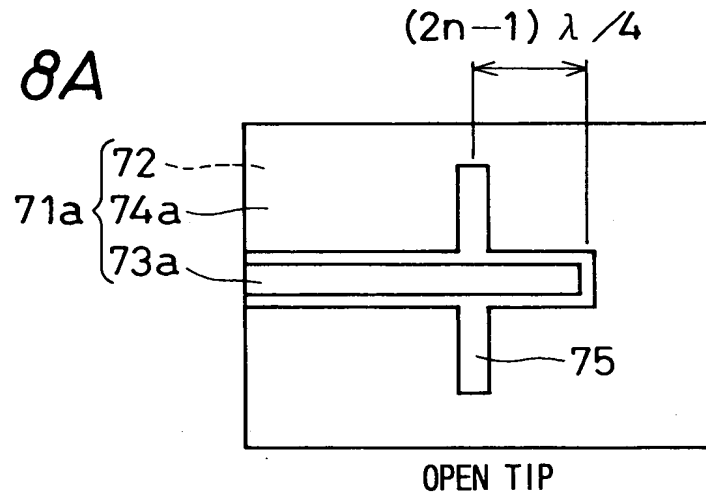
*FIG. 7A*



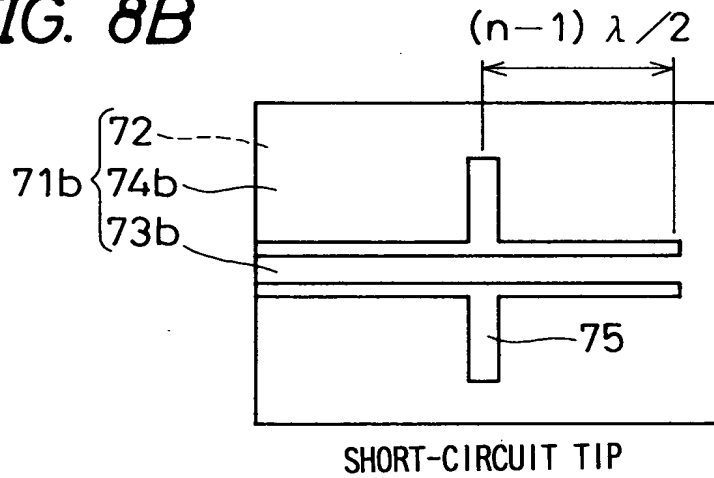
*FIG. 7B*



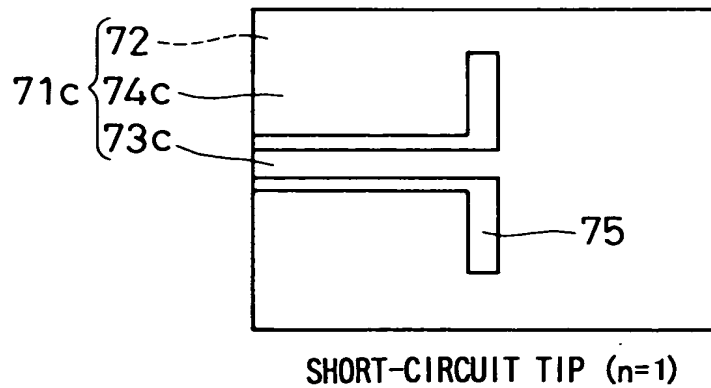
**FIG. 8A**



**FIG. 8B**

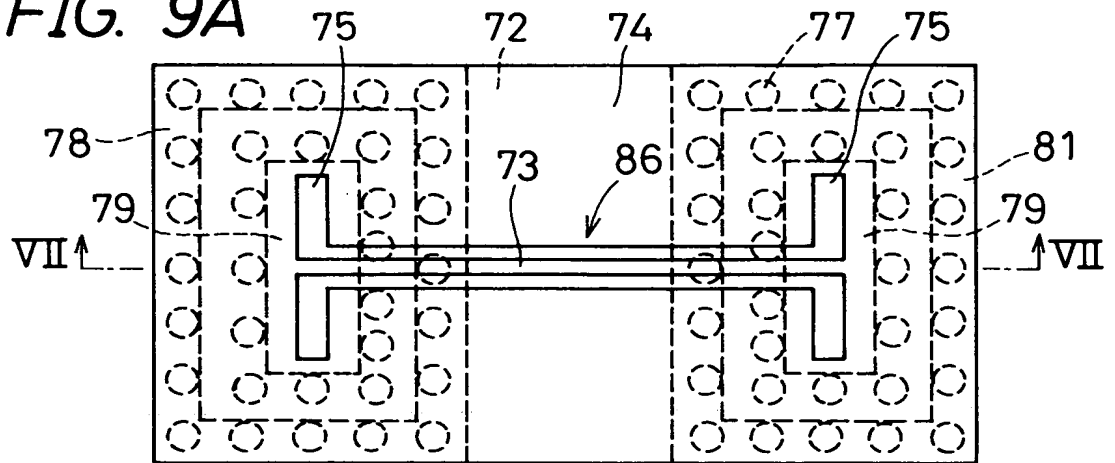


**FIG. 8C**

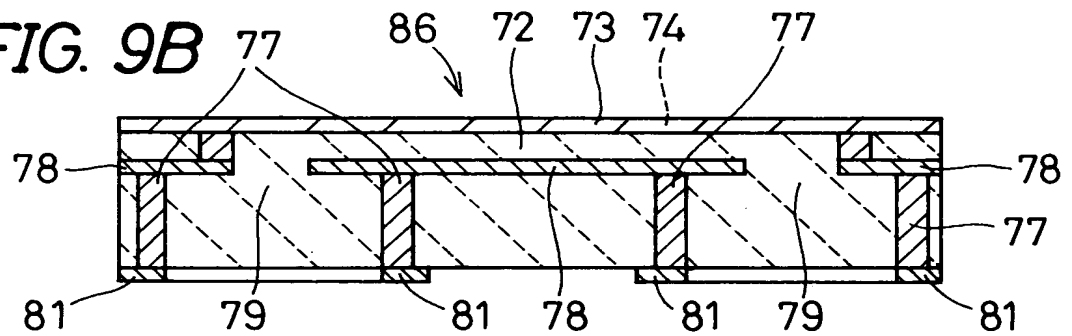




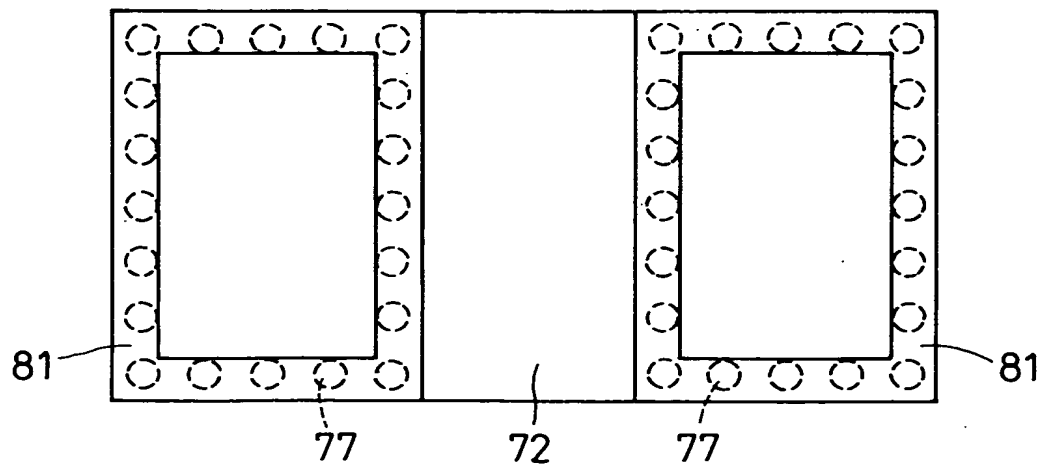
**FIG. 9A**



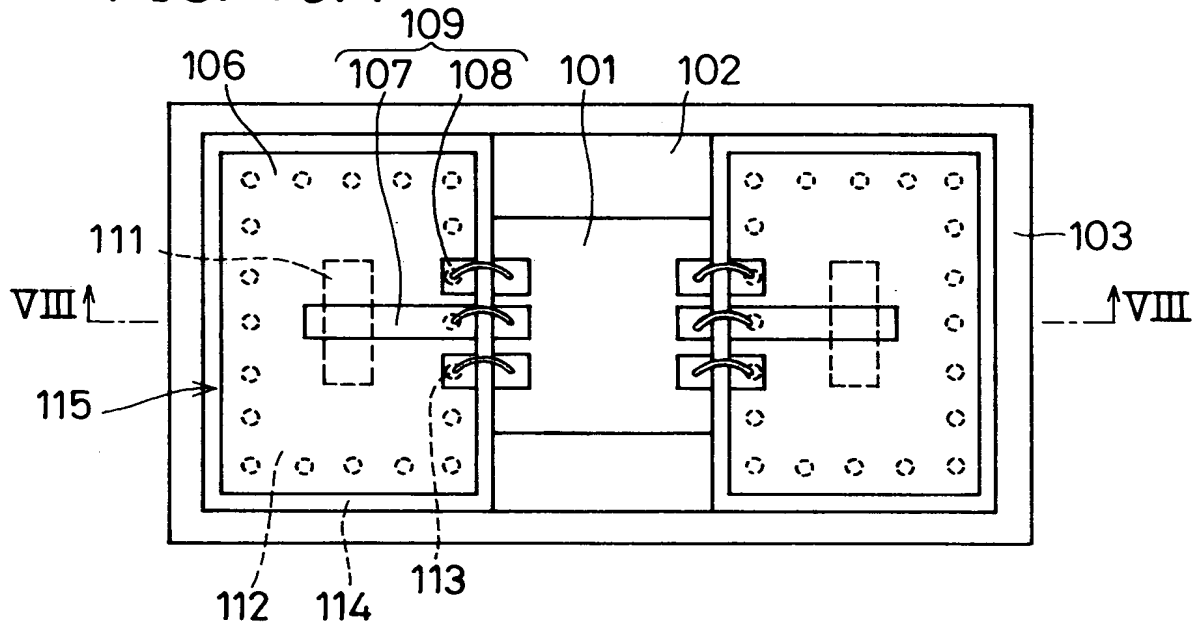
**FIG. 9B**



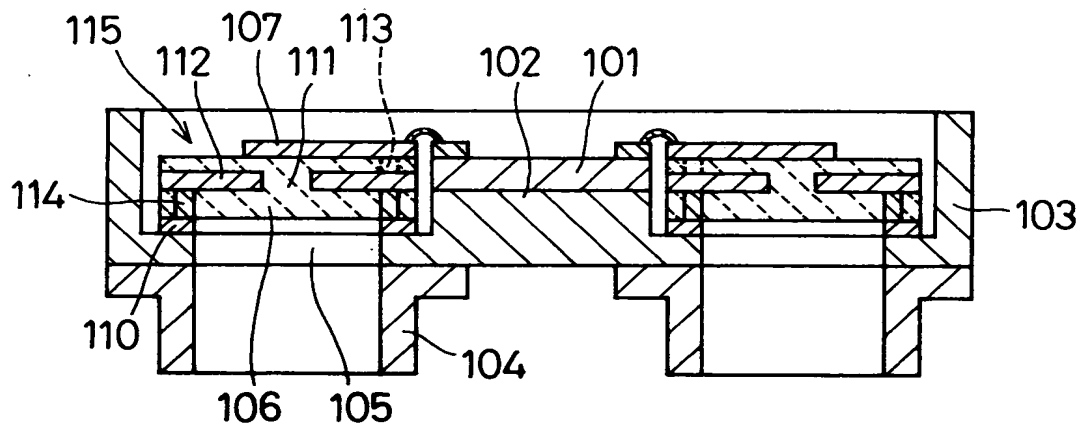
**FIG. 9C**



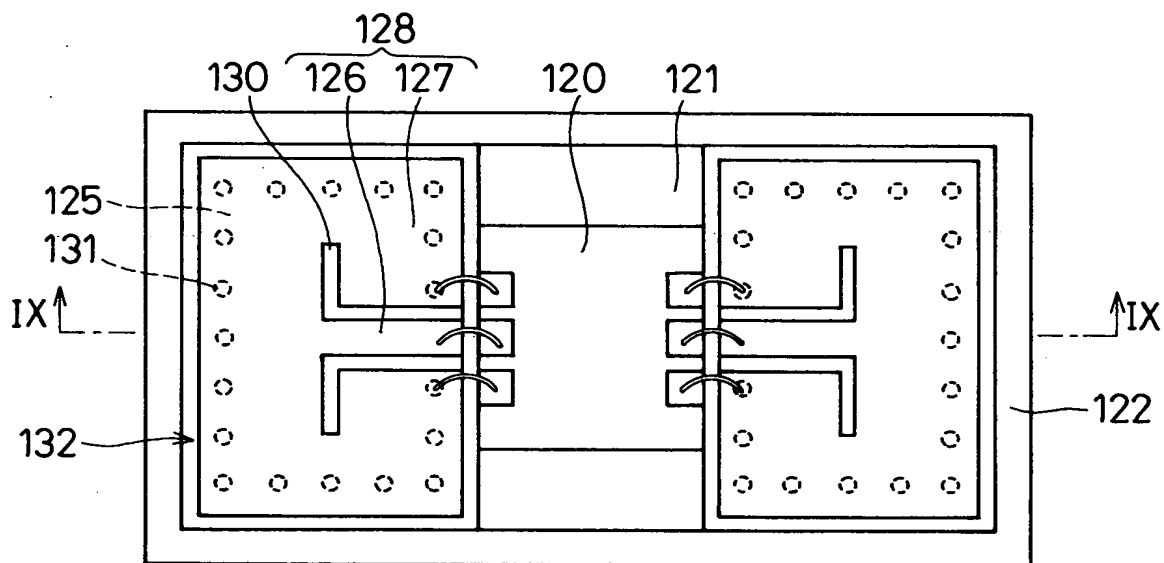
**FIG. 10A**



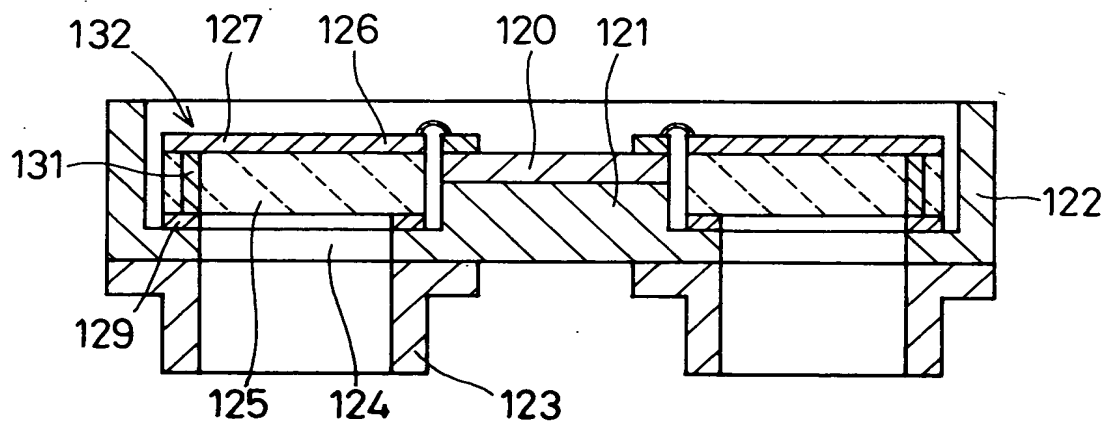
**FIG. 10B**



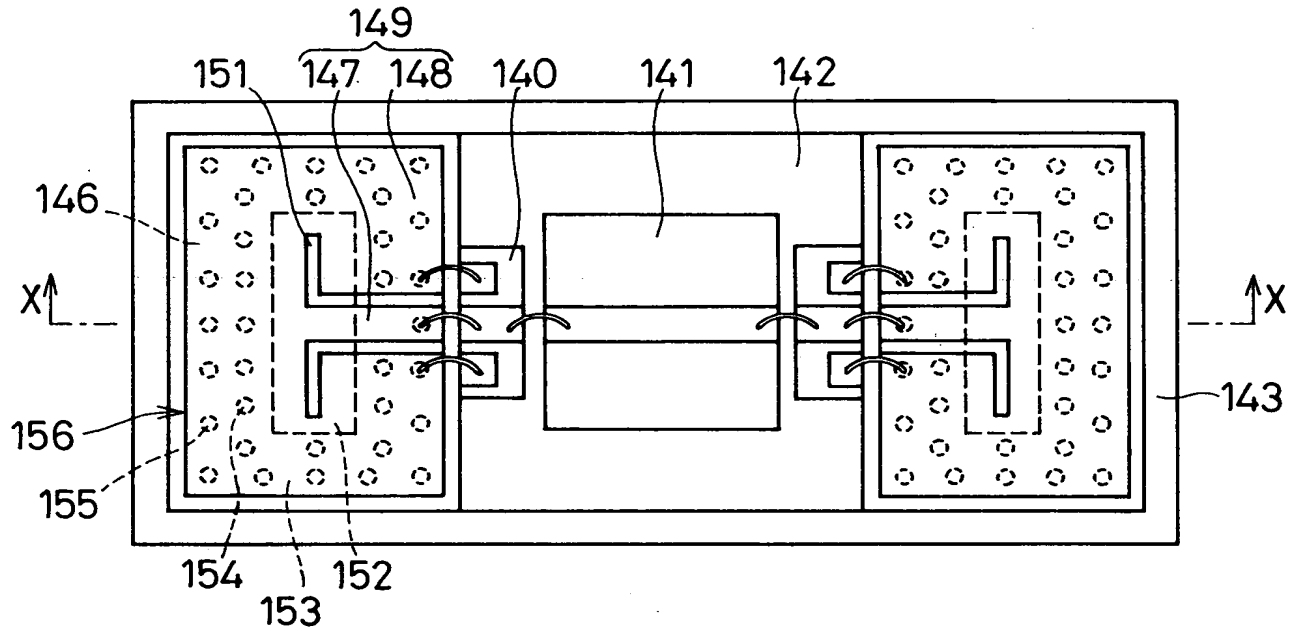
**FIG. 11A**



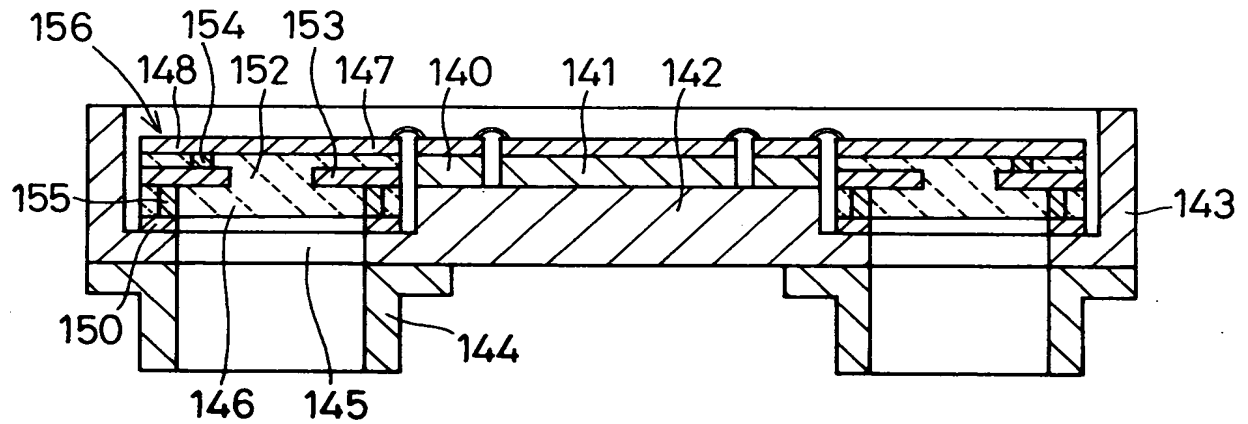
**FIG. 11B**



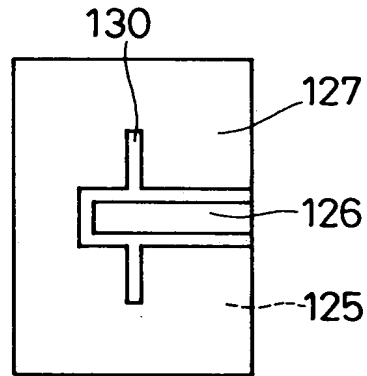
**FIG. 12A**



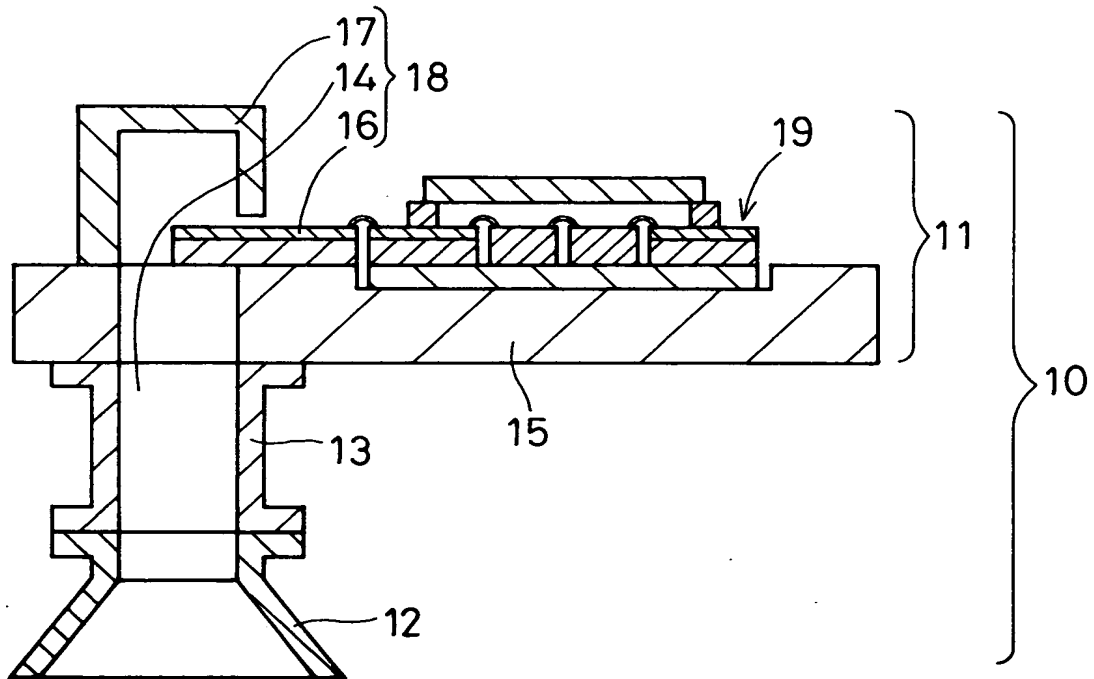
**FIG. 12B**



**FIG. 13**



**FIG. 14 PRIOR ART**



*FIG. 15 PRIOR ART*

